

THAT WHICH IS CLAIMED

1. A method for protecting an integrated circuit against piracy, characterized in that it comprises the successive steps, performed by the integrated circuit before a predetermined processing
5 sequence, of :

- detecting the state of at least one timer,
- controlling the activation timer if it is not activated, and
- disabling itself if the timer is activated.

2. A method according to claim 1, characterized in that it further comprises the step, performed by the integrated circuit if the predetermined processing sequence has been performed normally, of
5 deactivating the timer.

3. A method according to claim 1 or 2, characterized in that it further comprises the step, performed by the integrated circuit if it is detected that the timer is activated, of modifying the value of a
5 counter within a protected area in a non-volatile memory, comparing the counted value with a predefined threshold, and performing a processing for protecting confidential data stored within memories in the integrated circuit if the counted value reaches a predefined threshold.

4. A method according to claim 3, characterized in that said protection processing consists in erasing the confidential data from the memories in the integrated circuit.

10004527 10101

5. A method according to claim 3, characterized in that said protection processing consists in erasing a secret code stored within a memory in the integrated circuit.

6. A method according to claim 3, characterized in that said protection processing consists in erasing all memories in the integrated circuit.

7. A method according to any of claims 1 to 4, characterized in that, before performing a calculation of a sequence of a predefined number of calculations, the integrated circuit detects the state of a respective
5 timer, each calculation being associated with a respective timer, controls the activation of the associated timer if it is not activated, and disables itself if the associated timer is activated.

8. An integrated circuit protected against piracy, characterized in that it comprises at least one timer circuit comprising means for activating a timer designed to remain in an activated state as long as the
5 circuit is powered-on and for a predetermined duration if the circuit is powered-off, means for deactivating the timer, and means for detecting the activated or deactivated state of the timer; wherein the integrated circuit additionally comprises means for reading the
10 timer state, and for disabling itself at predefined times if the timer is in the activated state.

9. An integrated circuit according to claim 8, characterized in that it further comprises means for

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deactivating the timer after normal execution of a predetermined processing sequence.

10. An integrated circuit according to claim 8 or 9, characterized in that each timer circuit further comprises means for detecting the presence of the power supply, and means for allowing the timer to be activated
5 or deactivated when the power voltage is detected as present during a predetermined time period.

11. An integrated circuit according to any of claims 8 to 10, characterized in that it comprises a plurality of timer circuits, each timer circuit being associated with a calculation performed by the integrated
5 circuit, the integrated circuit comprising means for determining, before each calculation, the state of the timer associated with the calculation, activating the associated timer if it is not activated, and disabling itself if the associated timer is activated.

12. An integrated circuit according to any of claims 8 to 11, characterized in that each timer circuit comprises a capacitor associated with:

- a discharge circuit designed so that the
5 capacitor slowly discharges when the device is powered-off,

- a circuit for detecting capacitor charging,
- means for controlling capacitor charging,
and

10 - means for controlling capacitor discharging.

13. An integrated circuit according to claim 12, characterized in that the means for controlling

10004527 10101

14. An integrated circuit according to any of claims 8 to 13, characterized in that it comprises an MOS transistor having very small leakage currents, which is associated with the capacitor so that it is only
5 discharged by said leakage currents when the integrated circuit is powered-off.

15. An integrated circuit according to any of claims 8 to 14, characterized in that it comprises a test circuit, which is controlled by a test instruction, for reducing the timing duration.